REMARKS / ARGUMENTS

Claims 16-27 remain pending in this application. No claims have been canceled or added.

Priority

Applicants request acknowledgment of the claim for priority. The priority document was filed in the parent application and is cited in the Official Filing Receipt.

35 U.S.C. §102

Claims 16-27 stand rejected under 35 U.S.C. §102(b) as being anticipated by McDaniel et al (U.S. Patent No. 4,415,985). These rejections are traversed as follows.

The present invention is directed to a display apparatus as recited in claims 1, 21 and 26. Namely, the present invention is directed to a display apparatus that is connectable to an external computer, for displaying an image on a screen on the basis of video and synchronization signals from the external computer. The display apparatus includes a memory which is within the display apparatus, a receiver receiving a control signal to control the displayed image, which is generated by operating an input unit of the external computer, wherein the display apparatus is configured to be separate from the external computer, and a control circuit which

controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory. The control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

As such, as explained in the specification on page 4, lines 2-9, it is possible to adjust a display picture by an input unit such as a keyboard near at hand through a computer body and monitoring reception of a display control command without extending the hands to adjustment switches of a display unit, thereby easily and precisely obtaining a display state required by the user. In addition, as recited in the last paragraph of claim 1, the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

On the other hand, the cited reference, McDaniel et al., teaches a driving circuit for selectively displaying, on the screen of a cathode ray tube, a prespecified set of characters, wherein the characters are either displayed having a nominal size or displayed having a height that is twice that of the nominal size (see Fig. 30 showing a single unit control panel having a CRT, keyboards, and a control processor, and column 1, lines 6-15). Fig. 1 of McDaniel et al. shows a circuit structure of the single unit driving apparatus much different from the display apparatus of the present invention. The display apparatus of the present invention is connectable to an external computer, for displaying an image on a screen on the

basis of video and synchronization signals from the external computer which improves handling capability (See Specification page 1, line 9).

The above features of the present invention recited in claim 1 are neither disclosed nor suggested by McDaniel et al. Each of the Examiner's assertions will now be discussed in more detail.

As to independent claims 16, 21 and 26, the Examiner contends that McDaniel et al. disclose a display apparatus (Fig. 1, item 64) to an external computer (Fig. 1, item 50) for displaying and image on a screen on the basis of video and synchronization signal from the external computer (col. 6, lines 15-25), comprising; a memory (Fig. 1, item 6, column 3, lines 27-29, col. 4, lines 1-2) (underlining added).

It should be noted that item 60 PROM is within the single unit driving apparatus that is much different from the display apparatus of the present invention, which is connectable to an external computer. Further, by referring to McDaniel et al., column 3, lines 27-29, it can be clearly understood that the system 50 includes a PROM module 60 for storing the executive program of the system 50. On the other hand, the memory which is within the display apparatus according to the present invention stores the control data included in the control signal received through the receiver.

In addition, by referring to the comment that "these operations may include I/O read, I/O write, memory read, memory write", it can also be realized that any one or combination of "I/O read, I/O write, memory read, memory write" fails to disclose or suggest the feature that the control circuit reads control data from the memory when

the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory of the present invention (See McDaniel et al, col. 4, lines 1-2).

Next, the Examiner refers to a receiver which receives a control signal to control the image, which is generated by operating an input unit of the external computer (citing McDaniel at col. 5, lines 60-col. 6, lines 10, and col. 10, lines 24-39). However, the peripheral control 62 shown in Figs. 1 and 4 is within the single body apparatus wherein the CRT controller 158 receives data from the DMA controller 152, which is much different from the display apparatus of the present invention, which is connectable to an external computer, for displaying an image on a screen on the basis of video and synchronization signals from the external computer, or from the feature that the control circuit that reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory or the transmission of the data between the CRT controller 158 and the DMA controller 152.

The description at col. 5, line 60-col. 6, line 10 of McDaniel et al. disclose the following:

> The CRT controller logic 156 communicates with the DMA controller 152 and buffer 150. The CRT controller logic generates signals to be used by the cathode rate tube (CRT) 178. The DMA controller 152 controls the flow of data from the processor (computer memory) to the CRT control 158. The CRT controller 158 in turn requests and receives data from the DMA controller 152 and provides the necessary timing and control to right dot matrix characters on the face of the CRT 178. The CRT controller communicates with a bi-polar PROM which provides double height characters on the face of the CRT 178. A

> character PROM 166 provides storage of the predetermined set of dot matrix characters to be generated on the CRT 178.

However, what the CRT controller 158 provides and control here are characters to be written on the face of the CRT 178. Thus, McDaniel et al. are silent with respect to the control circuit that reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory. It should be noted that McDaniel et al. merely disclose the "address information" (col. 5, lines 54-60) sent from the DMA controller 152 thereby to read therefrom the dot matrix characters. The "address information" does not correspond to the control data or the control signal of the present invention.

The description at the above-cited col. 10, lines 24-39 of McDaniel et al states the following:

> Reference is now made to FIGS. 11 and 12. FIG. 11 illustrates a more detailed blocked diagram of the input module as illustrated in FIG. 10. The input signal module 82, as illustrated in FIG. 11, is designed to receive 32 machine input signals with 16 signals directed to the programmable interface controller 262 and with another 16 signals directed to another controller 264. These input signals may be generated by hardware, the machine tool or operator via a keyboard or other input device. In essence, the input signal module provides a means for the operator and machine to communicate with the processor module 52. An example of such signal is a signal indicating that a tool change operation has been completed. FIG. 12 illustrates a typical one of the input circuits within the buffer circuit 260 as well as one of the two input enable circuits 270 or 272. (underlining added)

It should be noted that the disclosure of "a signal indicating that a tool change operation has been completed" does not disclose or suggest a control circuit that

controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory as in the present invention. The image implies the display size, the display position or the brightness as recited in claim 27. Accordingly, the above col. 10, lines 24-39 of McDaniel et al. cannot teach the feature that the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

The Examiner next refers to the claimed control circuit which controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory and cites the following portion of McDaniel et al:

> The CRT controller logic 156 communicates with the DMA controller 152 and buffer 150. The CRT controller logic generates signals to be used by the cathode rate tube (CRT) 178. The DMA controller 152 controls the flow of data from the processor (computer memory) to the CRT control 158. The CRT controller 158 in turn requests and receives data from the DMA controller 152 and provides the necessary timing and control to right dot matrix characters on the face of the CRT 178. The CRT controller communicates with a bi-polar PROM which provides double height characters on the face of the CRT 178. A character PROM 166 provides storage of the predetermined set of dot matrix characters to be generated on the CRT 178. Each character line of the character PROM 166 is transferred to a shift register such as an 8-bit parallel input serial output register 168 which, in turn, shifts the information to the video input of the CRT 178 (See Col. 5, line 60 to Col. 6, line 10) (Underlining added).

In other words, from the description above, it can be seen that McDaniel et al. read or write dot matrix characters in the memory and transfer the data to the shift

register. However, they do not disclose or suggest the features of the present invention, as recited in claim 16 including:

a memory which is within the display apparatus;

a receiver receiving a control signal to control the displayed image, which is generated by operating an input unit of the external computer, wherein the display apparatus is configured to be separate from the external computer; and

a control circuit which controls the image on the screen using control data included in the control signal received through the receiver and writes said control data into said memory;

wherein said control circuit reads control data from said memory when said display apparatus is turned on and controls said displayed image on said screen by using the control data read out from the memory.

The Examiner refers to the Fig. 23 of McDaniel et al and the disclosure from col. 22, line 31 to col. 23, line 11, which states:

> Double size height character displays are provided to the CRT 178 by means of the decoder prom 164 and the attribute bits GPA0 and GPA1 which are generated by controller 158. The address of the decoded prom 164 can be subdivided into two portions. The lower significant four bits of address is applied by the line count signals of the CRT controller 158 and the upper significant bits of address are provided by the two general purpose attribute outputs from the CRT controller 158. The line counter outputs (D01-D04) of the decoder prom 164 are connected to the character prom 166 and serve to access the corresponding line number of the character dot array residing in the character prom 166. As an example, if the character code lines (CC0-CC6) from the controller 158 to the character prom 166 correspond to the row and column number for a capital letter "T" then the individual dot lines which are displayed on the screen to portray the "T" are addressed via the line

> counter signals (LC0-LC3) to the character prom 166. It should be noted that the two general purpose attribute bits GPA0 and GPA1 are reset and the contents of the decoder prom 164 and therefore the output of the character prom 166 correspond to the line counter input to the decoder prom 164. This procedure results in a single height character being displayed on the screen of the CRT 178. When the general purpose attribute bit 1 (GPA0) is set, the output of the decoder prom 164 is such that each character line within the character prom 166 is scanned twice for the character lines 0 through 5 while the line counter of the controller 158 steps through the lines 0 through 11. Consequently during one complete row of character display, only the first half of each selected character for that row will be scanned and presented on the CRT 178. When the next row is scanned the operating program sets the second general purpose attribute bit (GPA1) and GPA0 is reset thereby selecting the next scanning portion of the decoder prom 164. Note that during the addressing of the second row the line counter communicates to the decoder prom 164 to select row numbers 6 through 11 of the character prom 166. Again as with the previous row, each line of the character code is scanned twice thereby doubling the vertical size of the final character. At the end of the presentation of double height characters a field attribute code must be programmed so as to reset the general purpose attribute bits. If this is not done the lower half of the characters for the rest of the frame will be displayed on the screen with the upper half missing. (Underlining added).

Providing the double size height character displays merely means that the number of lines is made twice in a scanning control of character data. On the other hand, the present invention is directed to an adjustment of a display size, a display position and brightness of a picture in the display unit as explained in the present specification as follows:

> The present invention relates to an image display apparatus including an input unit such as a keyboard, a computer body and a display unit, and more particularly to an image display apparatus in which a display size, a display position and brightness of a picture in the display unit can be adjusted by the input unit such as the keyboard through the computer body to improve the handling capability. The image display apparatus of the present invention can be used in a work station and an advanced personal computer using a display unit (see Specification page 1, lines 2-12).

Therefore, McDaniel et al., in Fig. 23 and the accompanying description, do not disclose or suggest the claimed features of the present invention within the single unit driving apparatus, including:

a memory which has been within the display apparatus;

a receiver receiving a control signal to control the displayed image, which is generated by operating an input unit of the external computer, wherein the display apparatus is configured to be separate from the external computer; and

a control circuit which controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory;

wherein the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

The Examiner next refers to the claimed wherein clause stating that "wherein the control circuit reads control data from the memory when the display apparatus is turned on and controls the image on the screen by using the control data read out from the memory" and refers to McDaniel et al at col. 6, lines 28-58, reproduced below:

> In operation the CRT logic 156 is as follows. When initialized by an operating system command from the PROM 60 or processor 90 the CRT controller 158 requests DMA service from the DMA controller 152. As previously mentioned the DMA controller 152 activates a HOLD signal to the processor 90 which upon completing its current instruction switches the bus outputs to a high impedance condition thereby releasing the system buses to the DMA controller 152. The DMA controller 152 then provides addresses to the

> system's address bus 54 to access the system memory assigned for CRT 178 messages to be displayed. The DMA controller generates a memory read signal which causes the address memory word to place its contents on the data bus 56. The DMA controller 152 then generates a I/O write signal which causes the data bus 56 to be clocked into the CRT controller 158. The CRT controller 158 takes the character information provided to it from the DMA controller 152 and the data bus 56 and generates the necessary line signal commands and character codes to the decoder PROM 164 and character PROM 166 to effect the generation of the pre-specified series of dot characters on the face of the CRT 178. The CRT controller 158 may be of the type such as the Intel 8275 which contains a data bus buffer, read-write, DMA control logic, a character counter, display row counters, buffer input controller, buffer output controller, two eighty character FIFO buffers, a character FIFO line counter and raster timing and video control circuits. (Underlining added).

Namely, McDaniel et al. teach to display, at the time of initialization, messages on the CRT 178. As such, McDaniel et al. do not disclose or suggest the feature of the present invention that the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

The Examiner contends, on page 3 of the Office Action, that in col. 5, lines 60-col. 6, line 10, "the prior art of McDaniel et al. teach where the CRT controller generates signals to be used by the CRT and further receives data from the DMA controller and uses it in order to control the characters/images to be displayed on the CRT, therefore disclosing the limitation set forth by the instant application", Applicants respectfully disagree in that the CRT controller generates ASCII code signals necessary to access the PROM 166 (See McDaniel et al, col. 5, lines 66-col. 6, lines 4). The CRT controller 158 in turn requests and receives data from the DMA controller 152 and provides the necessary timing and control to right dot matrix

characters on the face of the CRT 178. The CRT controller communicates with a bi-polar PROM which provides double height characters on the face of the CRT 178. A character PROM 166 provides storage of the predetermined set of dot matrix characters to be generated on the CRT 178.

Therefore, McDaniel et al. clearly do not disclose or suggest the claimed feature of the present invention that the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory.

The Examiner further contends, on page 4 of the Office Action, that "the CRT controller further receives data from the DMA controller", Applicants respectfully disagree in that McDaniel et al. merely teach the "address information" (col. 5, lines 54-60) sent from the DMA controller 152 thereby to read therefrom the dot matrix characters. The "address information" does not correspond to the control data or the control signal of the present invention.

The Examiner still further contends, on page 4 of the Office Action, that "a 'signal' or 'image' of the present invention is one and the same as the 'character' disclosed by McDaniel. However, the presently claimed invention is not mainly directed to the "image" itself, but the feature that the control circuit reads control data from the memory when the display apparatus is turned on and controls the displayed image on the screen by using the control data read out from the memory (see independent claims claim 1, 21, 26).

Furthermore, the Examiner contends, on page 4 of the Office Action, that "McDaniel et al disclose in col. 6, lines 1-10 where the PROM stores the character information." However, Applicants contend that while the PROM 166 stores this character information, the PROM 166 cannot suggest the feature of a control circuit which controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory wherein the receiver receives a control signal to control the displayed image, which is generated by operating an input unit of the external computer. Furthermore, the present invention is directed to an adjustment of a display size, a display position and brightness of a picture in the display unit as described in the specification.

With regard to the Examiner's comment, on page 4 of the Office Action, that "applicant does not claim where the memory must be within the display apparatus", the claims have been amended to clearly state that the memory is within the display apparatus.

In addition, the Examiner contends that "McDaniel et al discloses where the display apparatus contains the memory which is shown by the EPROM in col. 5, lines 18-20". However, the claims recite:

a memory which is within the display apparatus; and

a receiver receiving a control signal to control the displayed image, which is generated by operating an input unit of the external computer, wherein the display apparatus is configured to be separate from the external computer.

The above claimed combination of the present invention cannot be taught by the circuit structure of the single unit driving apparatus of McDaniel et al.

Finally, Applicants wish to point out to the Examiner that the PROM 140 of McDaniel et al is programmed with the operating program of the control system 50 in a known manner to execute a set of determinable functions and serves to initialize the system's parameters (See Col. 5, lines 20-23). As such, the PROM 140 of McDaniel et al. is for storing the operating program (OS), which is far from both the object and the structure of the present invention directed to a display apparatus, which is connectable to an external computer, for displaying an image on a screen on the basis of video and synchronization signals from the external computer, comprising:

a memory which is within the display apparatus;

a receiver receiving a control signal to control the displayed image, which is generated by operating an input unit of the external computer, wherein the display apparatus is configured to be separate from the external computer; and

a control circuit which controls the image on the screen using control data included in the control signal received through the receiver and writes the control data into the memory.

While the language of claim 16 has been emphasized in these remarks, the remaining independent claims 21 and 26 contain similar limitations and are patentable for similar reasons. As such, it is submitted that all of the pending claims patentably define the present invention over the cited art.

Request for Interview

Applicants request that the Examiner conduct an interview with the undersigned to expedite prosecution of this application. As such, the Examiner is hereby invited to contact the undersigned by telephone to arrange an appropriate date and time for such interview.

Conclusion

In view of the foregoing, Applicants respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.

By_____
Shrinath Malur
Reg. No. 34,663
(703) 684-1120